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REMARKS

In the present Office Action, claims 1 - 7 were examined. Claims 8 - 18 are subject to restriction. Claims 1 - 7 are rejected. No claims are presently objected to or allowed.

By this Amendment, claims 1 and 3 - 7 have been amended, claims 2, 8 - 18 have been canceled. No new claims have been added. Accordingly, claims 1 and 3 - 7 are presented for further examination. No new matter has been added. By this Amendment, claims 1 and 3 - 7 are believed to be in condition for allowance.

Explanation of Above Amendments

In a paper mailed September 12, 2007, the Examiner requested restriction between the claims of Group I, claims 1-7, drawn to an integrated circuit device and the claims of Group II, claims 8-18, drawn to a method for singulating an integrated circuit. In a paper filed October 9, 2007, Applicants elected to prosecute the claims of Group I, claims 1-7, and traversed the restriction requirement. The Examiner has now repeated the restriction requirement and made it final. Applicants therefore confirm the election of the Group I claims, claims 1-7, and cancel claims 8-18 drawn to the non-elected embodiment.

Pending claims 1 and 3-7 have been amended to remove drawing figure reference numerals from the claims. Claim 1 has been further amended to recite that the sides of an integrated circuit (IC) encased in the claimed package are shaped to be effective to accomplish all of the following: (i) limit ingress of moisture along an interface between the IC and package; (ii) mechanically lock the IC to a molding resin forming the package body; and (iii) result in a backside surface of the IC having a smaller surface area than an opposing electrically active surface of the IC.

Applicants' invention, as embodied in claim 1 and illustrated in the Figure 2, is drawn to an integrated circuit device package capable of having a thickness, T, that does not much exceed the thickness of the integrated circuit device 12. An electrically active face 16 of the integrated circuit device 12 is electrically interconnected to a lead frame 20. A backside 14 of the

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integrated circuit device forms a portion of a surface of the package. Because this backside of the integrated circuit device forms the surface of the package, an interface 28 between the integrated circuit device and a molding resin likewise extends to a surface of the package. This generates issues impacting package reliability which do not exist when the integrated circuit device is completely encapsulated within a molding resin, as for example illustrated in the *Masumoto, et al.* patent (US 6,759,745) applied as a reference against certain of the claims of this patent application.

As best shown in Figure 2 of Applicants' application, the interface 28 is not a straight line, but rather an extended path. Further, because an interior portion of the interface projects outward towards the sidewalls of the integrated circuit package, molding resin extends over a portion of the surfaces forming the sides of the integrated circuit. As noted in amended claim 1, this feature leads to a number of beneficial results. First, the ingress of moisture along the interface is limited. Second, the molding resin extending over a portion of the integrated circuit device, mechanically locking the IC device into the molding resin (see the last sentence of paragraph [0024]). In addition, the surface area of the backside 14 is smaller than the surface area of the electrically active surface 16. Such features and the associated benefits are neither taught nor suggested by any of the references currently of record in the present application.

Applicants' claims 1, 2 and 4 were rejected under 35 USC 102(e) as anticipated by *Seo et al.* (US 6,858,919). Claim 2 has been cancelled without prejudice or disclaimer rendering the rejection of that claim moot.

*Seo et al.* disclose an integrated circuit package having an integrated circuit device with an electrically active face and an opposing backside face. The electrically active face is soldered to leads that extend through the package. While the backside 2c forms a surface of the package, the interface between molding resin 10 and integrated circuit device 2 is a straight line and does not include any feature effective to limit ingress of moisture and mechanically lock the integrated circuit device to the molding resin as claimed by Applicants in claim 1. Applicants' claim 1 and the claims dependent therefrom should be allowed over the *Seo et al.* reference.

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Applicants' claim 3 that recites the integrated circuit side feature includes two elements intersecting at an angle of approximately 90°, thereby forming a step-like structure, was rejected as obvious in view of the combination of *Seo et al.* in view of *Masumoto et al.* *Masumoto et al.* disclose at column 4, line 63 that the surface of the integrated circuit device that adheres to other features of the package is smaller than the opposing other side of the integrated circuit device. This is contrary to Applicants' embodiments, as illustrated in Applicants' Figure 2 where the surface 16 attached to other package features has a larger surface area than the opposing side. As disclosed in the Abstract to *Masumoto et al.*, the smaller surface is intended to limit fillet spread out around the semiconductor chip. It is further noted that in no embodiments of *Masumoto et al.* does any surface of the integrated circuit device form a portion of the package surface. As such, *Masumoto et al.* does not include an interface extending to a surface of the package.

*Masumoto et al.* teach away from Applicants' claims in that the surface of the integrated circuit device bonded to other features has a smaller surface area of than the opposing other side while in Applicants' claims the surface bonded to other features has a larger surface area than the backside that forms a portion for the package. Further, as *Masumoto et al.* do not have an interface extending to the package surface, there is nothing in the combination of *Seo et al.* and *Masumoto et al.* to teach or suggest features to limit the ingress of moisture along the interface and to mechanically lock the integrated circuit device to the dielectric molding resin. Applicants' claims should be allowed over the combination of references.

Applicants' claim 5 recites that the thickness of the package is approximately 0.01 inch. Claim 5 was rejected under 35 USC 103(a) as unpatentable over *Seo et al.* in view of *Kinsman*. (US 6,700,206). Applicants first note that the reference in *Kinsman* to 0.012 inch refers to the thickness of a conventional semiconductor die (see *Kinsman* at column 6, line 18) rather than the overall thickness of a package. As each embodiment of *Kinsman* appears to include wire bonds 34, it is not apparent that *Kinsman* teaches or suggests a package with a thickness of approximately 0.01 inch, rather, it is believed that the *Kinsman* packages would be considerably thicker. Applicants' claim 5 is believed to be non-obvious in view of the combination of *Seo et al.* and *Kinsman*.

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Applicants' claims 6 and 7 include a feature where the integrated circuit device is a sensor responsive to external stimulus, such as touch. Claims 6 and 7 were rejected under 35 USC 103(a) as unpatentable over *Seo et al.* in view of *Okada et al.* (US 7,192,789). It is acknowledged that *Okada et al.* disclose an integrated circuit device having a sensor part 4 that is sensitive to touch. However, the sides of the *Okada et al.* integrated circuit are straight and do not include any features effective to limit the ingress of moisture along an interface between the integrated circuit device and the molding resin nor to mechanically lock the integrated circuit device to the molding resin. As neither *Seo et al.* nor *Okada et al.* disclose such features as embodied in Applicants' claim 1, Applicants' claims 6 and 7, that depend from and further limit and define claim 1, should be allowed over the combination of references.

**CORRECTION OF FILING RECEIPT**

Applicants enclose a copy of a paper filed May 1, 2007 requesting correction to the filing receipt. Two corrections were requested. One was correction of the spelling of the name of inventor San Antonio and the second was to correctly identify the Applicant as a large entity. The corrected filing receipt mailed December 6, 2007 correctly spelled the name of the inventor, however the patent owner continues to be identified as a small entity. This is incorrect, Applicants' assignee is a large entity. It is noted that the filing fee acknowledged as received is correct for a large entity. Correction of the entity status is respectfully solicited.

As Applicants' claims are neither taught nor suggested by the references cited herein, either alone or in combination, Applicants' claims 1 and 3-7 should be deemed allowable.

Accordingly, Applicants submit that none of the references, alone or in combination, anticipate or make obvious the invention as presently claimed and that the application is now in condition for allowance. Therefore, Applicants respectfully request reconsideration and further examination of the application and the Examiner is respectfully requested to take such proper actions so that a patent will issue herefrom as soon as possible.

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If the Examiner has any questions or believes that a discussion with Applicants' attorney would expedite prosecution, the Examiner is invited and encouraged to contact the undersigned at the telephone number below.

Please apply any credits or charge any deficiencies to our Deposit Account No. 23-1665.

Respectfully submitted,  
Michael H. McKerreghan, et al.



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Date: February 13, 2008

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